

Stephen M. Plaza

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General Career Objectives I am looking for a full-time position requiring managing and technical expertise in one or more of the following areas: computer engineering, software development, software/hardware systems, advanced algorithms, bioinformatics, and semi-conductors. My diverse educational/work background in the semi-conductor industry, image processing, and neuro-anatomy along with my outgoing personality and project management experience enable me to be effectively deployed in multiple technical and managerial capacities. In particular, I seek employment in cutting edge technology and believe I am best able to contribute as a project lead.

Education	Certificate in Project Management, Georgetown	<i>August 2011</i>
	Ph.D. in Comp. Science and Eng, University of Michigan Ann Arbor	<i>May 2008</i>
	MSE Comp. Science and Eng, University of Michigan (GPA: 8.0)	<i>April 2004</i>
	B.S.E. Comp. Eng, University of Michigan (GPA: 3.9– <i>Summa Cum Laude</i>)	<i>April 2003</i>

Post-Grad Work Experience

- Janelia Farm Research Campus, Howard Hughes Medical Institute 2010-current
 - Project planning for cross-disciplinary teams
 - Computer vision algorithms to reconstruct the neural connectome
 - Programming and algorithmic contributions to scientific software
- Synopsys Implementation Group 2008-2010
 - Computer chip design optimization and software multi-threading
 - Technical contributions to cutting-edge industry tools
- Synopsys Advanced Technology Group (ATG) 2008
 - Research lab exploring advanced Electronic Design Automation(EDA) solutions

Teaching Experience¹ (2006-2008)

- EECS 381: Object-oriented programming (C/C++) (3 semesters)
 - Advanced class on programming paradigms in an industry setting
 - Setup/run discussion sections, setup projects, grading, accessible office hours
- EECS 478: Logic Synthesis (2 semesters)
 - Optimization of computer logic used in computer chips
 - Setup/run discussion sections, substitute lectures, setup projects, grading, accessible office hours

Course Background

- Grading: Introduction to Electronic Circuits (EECS 215) (2003)
- Relevant project management courses: Project Management Fundamentals, Risk Management, Business Strategy and Program Management
- Relevant math courses: applied honors calculus III, IV (Math 255, 256), discrete logic (EECS 203), linear algebra (Math 419), probability theory (Math 425), partial differential equations (Math 454)
- Relevant computer courses: electronic circuits and signal processing (EECS 206, 215), compilers/architecture (EECS 570, 573, 583), algorithms (EECS 586)

¹ All course numbers given refer to the University of Michigan course catalogue

- Programming Background**
 - Industry code experience
 - Synopsys: optimization algorithms and parallel programming for chip optimization (primary language: C)
 - Janelia Farm Research Campus: computer vision algorithms, web applications, database management, probabilistic computation, and visualization tools (languages: Python, C++, Matlab, Javascript)
 - Other: industry data models and databases—OpenAccess (Si2), EDA software—OAGear
 - Academic code experience
 - synthesis/placement tools: ABC & SIS (Berkeley), Capo (UCLA & Michigan)
 - SAT solvers (zChaff, MiniSAT)
 - quantum algorithm simulation: QuIDDPro (high-performance quantum circuit simulation)
 - linear arithmetic solver: Yices SMT Solver
- Professional Activities**
 - Past Conference/Journal Peer Reviews: DAC, TCAD, TODAES, TC
 - Active reviewer for TCAD
 - Technical Program Committee Member: GLSVLSI 2011
- Awards/Honors**
 - IWLS 2007 Programming Contest (2nd place)
 - ISPD 2008 Best Paper Award
 - Acceptance of patentable scientific contribution: Synopsys 2009
- Selected Publications**
 - "Multi-mode Redundancy Removal," S. Plaza, P. Saxena, T. Shiple, and P-H. Ho, ISQED, 2011.
 - "Optimizing Non-Monotonic Interconnect using Functional Simulation and Logic Restructuring," S. Plaza, I. Markov, and V. Bertacco, TCAD, 2009.
 - "Signature-based SER Analysis and Design of Logic Circuits", S. Krishnaswamy, S. Plaza, I. Markov, and J. Hayes, TCAD, 2009.
 - "Random Stimulus Generation using Entropy and XOR Constraints," S. Plaza, I. Markov, and V. Bertacco, pp. 664-669, DATE, 2008.
 - "Low-latency SAT Solving on Multicore Processors with Priority Scheduling and XOR Partitioning," S. Plaza, I. Markov, and V. Bertacco, IWLS, 2008.
 - "Node Mergers in the Presence of Don't Cares," S. Plaza, K-H. Chang, I. Markov, and V. Bertacco, pp. 414-419, ASP-DAC, 2007.
 - "Architecting a Reliable CMP Switch Architecture," K. Constantinides, S. Plaza, J. Blome, B. Zhang, V. Bertacco, S. Mahlke, T. Austin, and M. Orshansky, Vol.4, No. 1, Article 2, ACM Transactions on Architecture and Code Optimization, March 2007.